Electronic Version
Stylesheet Version v1.1.1

NON-VOLATILE MEMORY WITH INDUCED BIT LINES

Abstract

An electrically programmable non-volatile memory cell is provided. A semiconductor substrate is prepared. A pair of spaced apart source/drain (S/D) regions is defined on the semiconductor substrate. The spaced apart S/D regions define a channel region in between. A first dielectric layer such as silicon dioxide is disposed on the S/D regions. An assistant gate is stacked on the first dielectric layer. The assistant gate has a top surface and sidewalls. A second dielectric layer comprising a charge-trapping layer is uniformly disposed on the top surface and sidewalls of the assistant gate and is also disposed on the channel region. The second dielectric layer provides a recessed trough between the S/D regions. A conductive gate material fills the recessed trough for controlling said channel region.